



**(43) International Publication Date**  
**29 December 2004 (29.12.2004)**

## PCT

**(10) International Publication Number**  
**WO 2004/114563 A1**

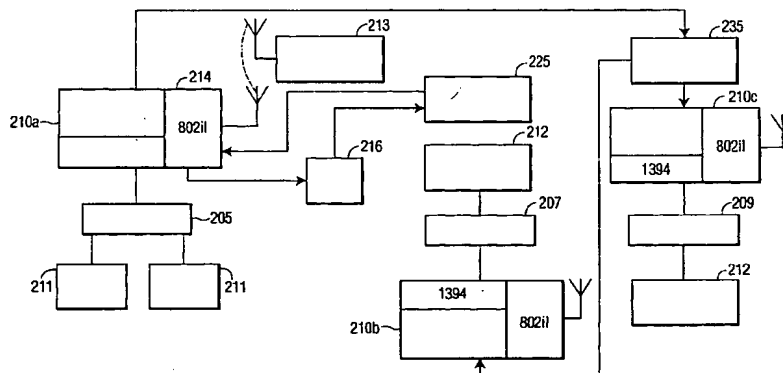
- (51) **International Patent Classification<sup>7</sup>:** **H04J 3/06,**  
H04L 12/28
- (21) **International Application Number:**  
PCT/IB2004/051004
- (22) **International Filing Date:** 24 June 2004 (24.06.2004)
- (25) **Filing Language:** English
- (26) **Publication Language:** English
- (30) **Priority Data:**  
60/482,654 26 June 2003 (26.06.2003) US
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- (81) **Designated States (unless otherwise indicated, for every  
kind of national protection available):** AE, AG, AL, AM,  
AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN,  
CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI,  
GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE,  
KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD,  
MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG,  
PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM,  
TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM,  
ZW.
- (84) **Designated States (unless otherwise indicated, for every  
kind of regional protection available):** ARIPO (BW, GH,  
GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM,  
ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM),  
European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI,  
FR, GB, GR, HU, IE, IT, LU, MC, NL, PL, PT, RO, SE, SI,  
SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ,  
GW, ML, MR, NE, SN, TD, TG).
- Declarations under Rule 4.17:**  
— as to applicant's entitlement to apply for and be granted  
a patent (Rule 4.17(ii)) for the following designations AE,  
AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ,  
CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE,

**Declarations under Rule 4.17:**

— as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii)) for the following designations AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE,

[Continued on next page]

- (54) Title:** METHOD FOR CLOCK SYNCHRONIZATION OF WIRELESS 1394 BUSES FOR NODES CONNECTED VIA IEEE 802.11 LAN



- (57) Abstract:** A method and apparatus for providing clock synchronization of 1394 buses having wireless devices utilizing 802.11 communication with computers attached to one or more 1394 buses, includes the steps of (a) synchronizing an internal time base of a wireless master device attached to a first bus by receiving a Software Beacon Alert that indicates a time of a subsequent transmission, applying the Software Beacon Alert to a first phase-lock loop circuit associated with the master device to create a filtered Software Beacon Alert. The first phase-lock loop circuit is unsymmetrical about zero error. A timing message is transmitted from the master device to a second phase-lock loop circuit associated with at least one slave device. The timing message must be sent to the at least one slave device before the master device receives a subsequent Software Beacon Alert message, so that the wireless master device and the at least one slave device are synchronized, even though they are on different buses. This invention allows 1394 devices having wireless means to communicate over an 802.11 WLAN network, so that communications can be synchronized between the master and slave device across 1394 serial buses.

**WO 2004/114563 A1**



EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, UZ, VC, VN, YU, ZA, ZM, ZW, ARIPO patent (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE,

IT, LU, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG)

— as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii)) for all designations

**Published:**

— with international search report

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

METHOD FOR CLOCK SYNCHRONIZATION OF WIRELESS 1394 BUSES FOR NODES CONNECTED VIA  
IEEE 802.11 LAN

5           The field of the invention relates to the synchronization of devices specified in standards such as IEEE 1394. More particularly, the present invention relates to the synchronization of IEEE 1394 devices connected via 802.11a or 802.11b wireless standards.

          IEEE 1394 is a standard for a serial bus wherein the devices are normally  
10   connected via a serial cable. For example, a camcorder, camera, or monitor can be connected with a first computer via a 1394 bus. The first computer will in all likelihood have a 1394 adapter card plugged into one of its slots to control and translate communications between the 1394 devices and the computer.

          However, with the advent of 802.11 radio, it is possible to have in a single  
15   device, such as computer, an 802.11 adapter card and a 1394 card that permits control of devices, for example, such as a camera, camcorder, monitor, etc. Another computer can communicate with the first computer, and if it is desired, for example, the images captured by the camera can be sent to the second computer. In order to send the images to the second computer, the camera will transfer image data along the 1394 wired bus to  
20   the first computer. With the advent of wireless communication, particularly WLAN such as 802.11a or 802.11b (hereinafter "802.11a/b") increases the possibility for this particular method of communication to be used for communication between the first and second computers.

          In order for 1394 devices attached to a 1394 bus to communicate with other  
25   1394 devices on another bus via wireless communication such as 802.11, most of the 1394 standards must be replicated in order to provide full 1394 functionality. The

synchronization of devices conventionally connected is specified in the IEEE 1394 standard, and a method for achieving this function in the European wireless standard entitled "Hiperlan" in ETSI TS 101 493-3.

However, there is no known method for synchronizing 1394 devices on different  
5    hardwired buses that attempt communication over 802.11a/b.

The synchronization issue is critical because devices using the 1394 standard use a synchronous system for timing. Although the 802.11a/b standards have a beacon, transmitted at regular intervals, the transmission or reception of this beacon is not directly accessible outside the 802.11a/b device. A computer does have access to the  
10    Software Beacon Alert (SBA). This alert is an indication from the 802.11a/b device that the beacon will be transmitted shortly and that software must prepare the beacon data. In addition, this alert can not be used directly for synchronization since it has a large (100us is not unusual) variability in delay from the 802.11a/b timebase. The target beacon transition time (TBTT) is used in 802.11 by the Point Coordinator (PC) to let  
15    devices know what is the time space between transmitted frames, with time being divided into repeated periods called superframes. A superframe begins with a beacon frame that permits the delivery of protocol parameters and allows for synchronization of the local timers in the stations. Thus, every station connected in the 802.11 network knows when the next beacon frame will arrive, which is announced in the beacon frame.

20       802.11a/b both utilize beacons transmitted at a constant rate, but the 802.11a/b is a non-synchronous protocol. Further complicating the problem is that the 802.11 is essentially divided into an adapter card (having the radio) and the computer to which it is connected (having the "smarts" necessary for control), and the card must generate an interrupt to be serviced by the computer.

Thus, the need exists to provide an accurate (i.e. clean) wall clock that could be used by the all the 802.11a/b devices to permit communication of devices attached on different 1394 buses.

The present invention provides a method and apparatus for synchronizing 1394  
5 devices that connect via an 802.11a/b WLAN.

According to a first aspect of the present invention, a first step of a two-step process that utilizes a first Phase Lock Loop (PLL) is used to provide a clean wall clock that can be used to synchronize the communications of the 1394 buses.

According to a second aspect of the present invention, a second step of a two step  
10 process is to transfer the cycle time information from a first 1394 bus 205 (shown in Fig. 2) to computer slave devices 210b and 210c, where the computer slave device 210b contains a second PLL.

Thus, the present invention permits synchronizing an internal time base to the SBA, and using the time base to synchronize 1394 buses.

15 Fig. 1 is a flowchart providing an overview of an aspect of the present invention.

Fig. 2 shows one way that an apparatus according to the present invention can be arranged.

According to the present invention, a digital phase lock loop (PLL) can be employed to provide a synchronization of the 802.11 devices attached to respective  
20 1394 buses with the following difference: the phase gain is not symmetrical about zero error.

Figure 1 illustrates an overview of a method according to the presenting invention. The process comprises two steps.

At step 110 an internal time base is synchronized to the Software Beacon Alert by applying the Software Beacon Alert to a first phase-lock loop (PLL) circuit that is unsymmetrical about zero error. The phase gain as used is typically not a straight line (linear) gain throughout. For example, a gain that is a small and constant value  
5 indicates a late beacon. However, a gain that is a large and proportional (linear) indicates that the beacon is early.

The Software Beacon Alert provides the time of the next beacon frame, which is referred to as target beacon transition time (TBTT). However, as previously disclosed, the Software Beacon Alert often incurs delays, which makes it unsuitable as a timing  
10 reference by itself. The time variation of the Software Beacon alert is almost always delayed to some degree. The present invention compensates for the time variation of the Software Beacon Alert by utilizing a PLL having a phase detector gain that is constant and small when the Software Beacon Alert is late, but large and proportional when the Software Beacon alert is early. This function is implemented identically on all  
15 wireless 1394 devices connected to the bus, giving them all a common, stable time base, by which to synchronize device hardwired to different buses.

At Step 120, the synchronized internal time base, which has been synchronized to the time of the Software Beacon Alert, is used to sample the cycle time of a 1394 adapter card of one of the computers and designate that particular card to be the cycle  
20 master. The cycle master samples the 1394 timebase in response to the filtered Software Beacon Alert. The master then transmits this time to all other wireless 1394 devices in a unique message. The time that it takes to transmit this time to the other devices is not critical, so long as it is transmitted by the next Software Beacon Alert since the time it was acquired is known to all wireless 1394 devices.

At step 130, the remaining devices, which are slaves, apply the timing messages received from the master to a second PLL. This use of a second PLL allows for error checking and limits the instantaneous change in the 1394 cycle time to a  $\pm 1$  clock per 1394 cycle. The slave devices 210b, 210c each have their own PLL circuit 225 (not shown) but arranged similar to that of the first PLL 225 of the master device 210a. It should be noted that the typical error between the master and slave only will be a portion of one clock per 1394 cycle. The PLL on the slaves must account for this error and distribute it evenly over many 1394 cycles. For example, a slave whose 24.576 MHz clock is a  $1/2$  clock per cycle slow would mean that every other cycle comprises 3071 clocks instead of the normal 3072.

Fig. 2 illustrates one way that a wireless system according to the present invention can be arranged. The buses 205, 207, 209 are 1394 buses. Devices 210a, 210b, 210c, are typically computers with 1394 adapter cards. The computers also have means for wireless communication 214 with WLAN devices 213, such as cameras 212, telephones (not shown), monitors 211, etc. In the present example, it is presumed that the wireless standard is 802.11, but other wireless forms of communication can be used.

Device 210a is designated as the master device, and devices 210b and 210c are the slave devices. The first phase-locked loop (PLL) 225 receives the Software Beacon Alert 216. The first PLL 225 is preferably a digital PLL that is not symmetrical about zero error. The gain of first PLL 225 is constant and small when the Software Beacon Alert is later than the announced arrival, but is large and proportional when the Software Beacon Alert is early. This function is implemented identically on all 1394 wireless devices, giving them a common, stable time base. The slave devices, 210b and 210c apply the time messages received from the master to the second PLL 235. The second

PLL 235 checks for the error on the master and distributes the error over many 1394 cycles.

Thus, all the 802.11a/b devices are synchronized to the same 1394 master device, even though they are connected to different buses. Every time a filtered interrupt  
5 occurs, the cycle time can be read out. Typically there is about 1ms to transfer the reading from the 802.11 cards. This reading is used on the next software alert. The slave side gives us a delta reading in addition to the delta reading from the master 1394 card, which allows the determination as to whether or not the timing is fast or slow. A standard PLL can be used to determine this timing, by comparing the cycle time with a  
10 local cycle time. Thus, the difference in timing can be corrected over a predetermined period of time to get the phase correct.

Various modifications can be made to the present invention that would not depart from the spirit of the invention, or the scope of the appended claims. It should be understood that the illustrations were provided for explanatory purposes and not to limit  
15 the claimed invention. Although the examples shown used computers having 1394 adapter cards and 802.11 cards to communicate with other wireless devices, it is possible that other types of devices can be attached to the 1394 bus, and the types of wireless device can be anything that can communicate with the device attached to the 1394 bus.



## Claims:

1. A method for clock synchronization of a plurality of wireless devices (213) that are in communication with respective nodes, wherein at least some of the respective nodes are attached to different buses, comprising the steps of:
  - 5 (a) synchronizing an internal time base (step 110) of a wireless master device (210a) attached to a first bus (205) by receiving a Software Beacon Alert (216) that indicates a time of a subsequent transmission and applying the Software Beacon Alert to a first phase-lock loop circuit (225) associated with the master device (210a) to create a filtered Software Beacon Alert, wherein said first phase-lock loop circuit (225) uses a  
10 phase detector with an asymmetrical gain about zero error;
  - (b) receiving a timing message (step 120) transmitted from the master device (210) on the first bus (205) to a second phase-lock loop circuit (235) associated with at least one slave device (210b, 210c) attached to one of a second bus (207) and a third bus (209) respectively of a plurality of buses; and
  - 15 (c) providing the timing message (step 130) from the second phase-locked loop (235) to said at least one slave device (210b, 210c) attached to said one of a second bus and a third bus before the master device (210a) receives a subsequent Software Beacon Alert message, so that the wireless master device (210a) and the at least one slave device (210b, 210c) are synchronized.
- 20 2. The method according to claim 1, wherein the timing message received in step (b) is error checked.
3. The method according to claim 2, wherein the instantaneous change in cycle time for the at least one slave device is limited to +/- one clock pulse per 1394 cycle.

4. The method according to claim 1, wherein the messages transmitted and received between the wireless master device (210a) and the at least one slave device (210b, 210c) utilize an 802.11 WLAN network.

5

5. The method according to claim 1, further comprising:

(d) determining whether the SBA is late or early by determining an output of the first phase lock loop circuit (225), wherein a constant value that is small relative to a predetermined value indicates that the SBA is late, whereas a relatively larger and proportional gain of the first phase lock loop circuit (225) indicates that the SBA is early.

6. A system for clock synchronization of wireless nodes, comprising:  
a master device (210a) attached to a first bus (205) having means for receiving a Software Beacon Alert (216) and means for communication (214) with at least one wireless device (213), said Software Beacon Alert providing an indication of a time of a subsequent transmission;

a first phase-lock loop device (225) in communication with the master device (210a), said first phase-lock loop device (225) being unsymmetrical about zero error so that a phase detector gain is constant and relatively smaller when the Software Beacon Alert is later than an indicated subsequent transmission time, and relatively larger and proportional when the Software Beacon Alert is earlier than the indicated subsequent transmission time, said first phase locked-loop providing a filtered Software Beacon Alert message;

at least one slave device (210b, 210c) that receives the filtered Software Beacon Alert message transmitted by the master device; said at least one slave device includes means for wireless communication (214) with at least one wireless device (213); and

a second phase-lock loop device (235) that is in communication with the at least  
5 one slave device (210b, 210c), said second phase-lock loop device is unsymmetrical about zero error so that a phase detector gain is constant and relatively smaller when the filtered Software Beacon Alert message is later than the indicated subsequent transmission time, and relatively larger and proportional when the Software Beacon Alert message is earlier than the indicated subsequent transmission time, so that said  
10 master device (210a) of the first bus and said at least one slave device (210b, 210c) of the second bus are synchronized.

7. The system according to claim 6, wherein the filtered Software Beacon Alert message received by the second phase-lock loop device (235) is error checked.

15

8. The system according to claim 7, wherein the instantaneous change in cycle time for the filtered Software Beacon Alert message of said at least one slave device (210b, 210c) is +/- one clock cycle.

20

9. The system according to claim 8, wherein the messages transmitted and received between a first wireless device (213) in communication with the master device (210a) and a second wireless device (215) in communication with at least one slave device (210b, 210c) utilize an 802.11 WLAN network.

25

10. The system according to claim 6, wherein the master device (210a) and the at least one slave device (210b, 210c) conform to the IEEE 1394 device timing

standards, and said master device (210a) and said at least one slave device (210b, 210c) are connected to respective 1394 serial buses.

11. The system according to claim 10, further comprising a plurality of IEEE  
5 1394 serial buses, with said master device (210a) being attached to a first of the plurality of IEEE serial buses and said slave device being attached a second of the plurality of IEEE 1394 buses.

12. An apparatus for receiving a Software Beacon Alert from a wireless  
10 network and synchronizing a plurality of wireless nodes, said apparatus comprising:

means for synchronizing a Software Beacon Alert that indicates a subsequent transmission time including a phase-lock loop filter (225) that is unsymmetrical about zero error, so that a phase detection gain is constant and relatively smaller when the Software Beacon Alert (SBA) is later than the indicated subsequent transmission time,  
15 and larger and proportional when the SBA is earlier than the indicated subsequent transmission time, said means for synchronizing providing a filtered Software Beacon Alert;

a master-slave arrangement (210a, 210b, 210c,) wherein a master device (210a) transmits a filtered Software Beacon Alert to at least one slave device (210b, 210c); and  
20 wherein each of said master device 210a and at least one slave device (210b, 210c) are attached to a respective 1394 serial buses, and each of said master and the at least one slave device having wireless communication with an 802.11 capable wireless device (213); and

a second phase-lock loop filter device (235) for said at least one slave device (210b, 210c) that performs error checking.

13. The apparatus according to claim 12, wherein the second phase-lock  
5 loop filter device (235) limits an instantaneous change to +/- one clock cycle.

14. The apparatus according to claim 12, wherein the second-phase lock  
loop filter device (235) distributes the instantaneous change over a plurality of cycles.

10 15. The apparatus according to claim 12, comprising at least an additional  
second phase-lock loop device (235) so that each respective slave device (210b, 210c)  
has a respective second phase-lock loop device.

16. The apparatus according to claim 12, wherein said wireless device  
15 communicating with said master device (210a) and the at least one slave device (210b,  
210c) communicate via an IEEE 802.11 protocol.

17. The apparatus according to claim 12, wherein the master device (210a)  
and the at least one slave device (210b, 210c) comprise computers having 1394 adapter  
20 cards to communicate with a 1394 serial bus, and 802.11 adapter cards for wireless  
transmission with 802.11 devices.

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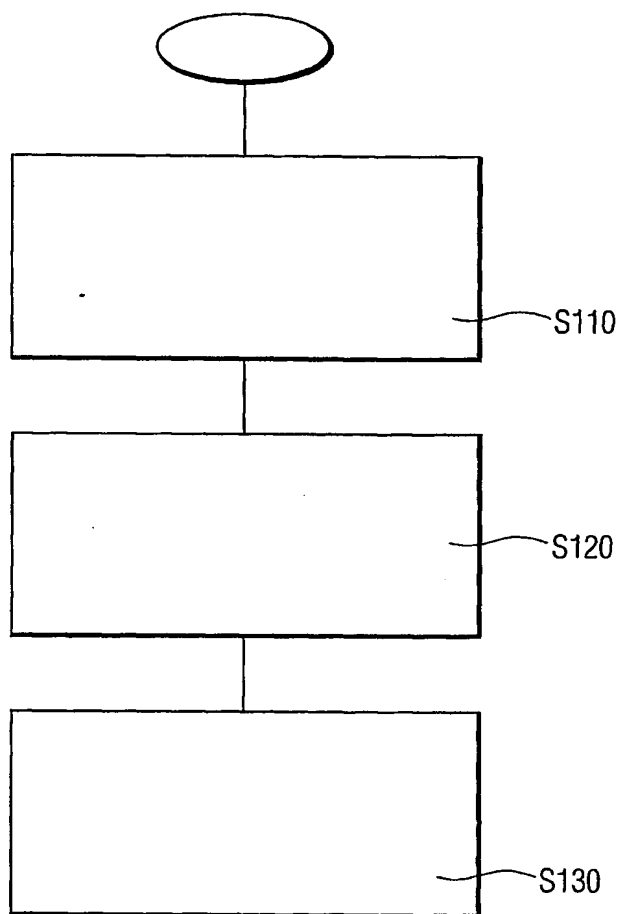


FIG. 1

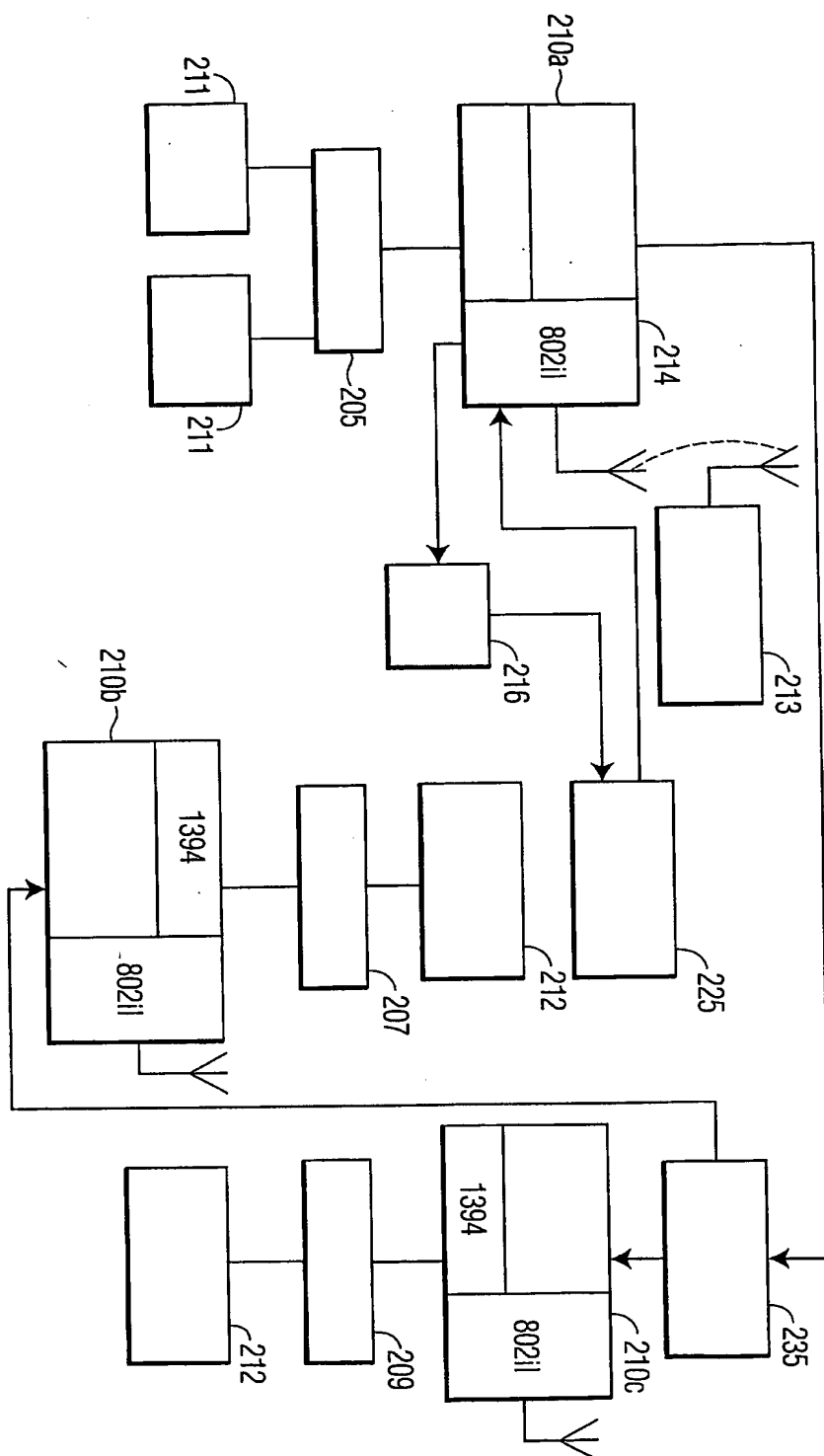


FIG. 2

# INTERNATIONAL SEARCH REPORT

International Application No  
T/IB2004/051004

**A. CLASSIFICATION OF SUBJECT MATTER**  
IPC 7 H04J3/06 H04L12/28

According to International Patent Classification (IPC) or to both national classification and IPC

**B. FIELDS SEARCHED**

Minimum documentation searched (classification system followed by classification symbols)  
IPC 7 H04J H04L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the International search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data, PAJ

**C. DOCUMENTS CONSIDERED TO BE RELEVANT**

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 99/55028 A (THOMSON MULTIMEDIA SA ; DORE RENAUD (FR); LOPEZ PATRICK (FR); STRAUB G) 28 October 1999 (1999-10-28) page 5, line 27 - page 6, line 16 page 10, line 32 - page 11, line 37 page 13, line 1 - page 13, line 18	1-17
A	US 2002/114303 A1 (BATES PHILIP M ET AL) 22 August 2002 (2002-08-22) paragraphs '0042! - '0045! figures 1,2	1,6,12

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

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Date of the actual completion of the International search

30 August 2004

Date of mailing of the International search report

08/09/2004

Name and mailing address of the ISA

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# INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No

T/IB2004/051004

Patent document cited in search report		Publication date	Patent family member(s)	Publication date
WO 9955028	A	28-10-1999	AU 3425399 A	08-11-1999
			CN 1297633 T	30-05-2001
			DE 69910558 D1	25-09-2003
			DE 69910558 T2	17-06-2004
			EP 1207641 A2	22-05-2002
			EP 1074104 A1	07-02-2001
			ES 2205806 T3	01-05-2004
			WO 9955028 A1	28-10-1999
			JP 2002512476 T	23-04-2002
US 2002114303	A1	22-08-2002	WO 02065707 A2	22-08-2002